THIS OPINION WAS NOT WRITTEN FOR PUBLICATION

The opinion in support of the decision being entered today (1) was not written for publication in a law journal and (2) is not binding precedent of the Board.

Paper No. 24

UNITED STATES PATENT AND TRADEMARK OFFICE

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BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

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Ex parte THEODORE C. WALDRON, III,
PAUL P. GIANGARRA,
KHOA D. HUYNH,
JOHN G. TYLER, and
SCOTT L. WINTERS

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Appeal No. 96-2160
Application 07/862,888[1]

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ON BRIEF

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Before KRASS, JERRY SMITH, and CARMICHAEL, Administrative Patent Judges.

JERRY SMITH, Administrative Patent Judge.

[1] Application for patent filed April 3, 1992.

DECISION ON APPEAL

This is a decision on the appeal under 35 U.S.C. § 134 from the examiner's rejection of claims 1-8, which constitute all the claims remaining in the application. An amendment after final rejection was filed on February 27, 1995 and was entered by the examiner.

The disclosed invention pertains to a method and apparatus for optimizing the dispatch latency of tasks in a data processing system. More particularly, a normal and expedited scheduling path are provided for scheduling tasks to be run on the processor. The normal or expedited scheduling path is selected based on the relationship between the task currently being executed and a task selected for execution.

Representative claim 1 is reproduced as follows:

1. A method of enhancing task scheduling efficiency in a data processing system having a processor, a memory, and a multitasking operating system for managing the processor and the memory, the method comprising the data processing system implemented steps of:

providing both a first expedited task scheduling path for tasks and a second task scheduling path for tasks in a scheduler within said multitasking operating system;

assigning an execution priority to each of a plurality of tasks within said data processing system for execution on the processor;

periodically placing selected tasks in a ready-to-run queue within said data processing system;

periodically selecting a task holding a highest execution priority from among said selected tasks in the ready-to-run queue;

determining if a task is executing on the processor;

if a task is executing on the processor, comparing the execution priority of the selected task to the execution priority of the executing task;

responsive to the selected task holding a higher execution priority or to absence of an executing task, processing the selected task for execution on the processor along said first expedited scheduling path; and

processing the selected task for execution on the processor along said second scheduling path responsive to the presence of an executing task holding an execution priority higher than the selected task.

The examiner relies on the following reference:

Deitel, An Introduction to Operating Systems, Addison-Wesley Publishing Company, Inc., pages 784-823, copyright 1990.

Claims 1-8 stand rejected under 35 U.S.C. § 102(b) as being anticipated by the disclosure of Deitel.

Rather than repeat the arguments of appellants or the examiner, we make reference to the briefs and the answer for the respective details thereof.

OPINION

We have carefully considered the subject matter on appeal, the rejection advanced by the examiner and the evidence of anticipation relied upon by the examiner as support for the rejection. We have, likewise, reviewed and taken into consideration, in reaching our decision, the appellants' arguments set forth in the briefs along with the examiner's rationale in support of the rejection and arguments in rebuttal set forth in the examiner's answer.

It is our view, after consideration of the record before us, that the disclosure of Deitel does fully meet the invention as set forth in claims 1-8. Accordingly, we affirm.

Anticipation under 35 U.S.C. § 102 requires that each element of the claim in issue be found, either expressly described or under principles of inherency, in a single prior art reference. Kalman v. Kimberly-Clark Corp., 713 F.2d 760, 771, 218 USPQ 781, 789 (Fed. Cir. 1983), cert. denied, 465 U.S. 1026 (1984). The examiner has indicated how he reads each of the claims on the disclosure of Deitel [answer, pages 2-5]. Appellants argued the claims as a single group in the original brief, and their only argument was that there was no "provision of a first expedited task scheduling path and a second task scheduling path within *Dietel* [sic] in the manner which is expressly set forth within these claims" [brief, page 7]. The examiner responded that the preemptive

scheduling path and the non-preemptive scheduling path of Deitel met the two paths argued and claimed by appellants [answer, page 5]. Appellants filed a reply brief in which they asserted that the claims had not been properly interpreted within the meaning of the sixth paragraph of 35 U.S.C. § 112.

We consider this latter argument first. In our view, method claim 1 is not written in "step plus function" form, but rather, is written as a conventional method. Claim 1 recites a simple sequence of steps, and the steps do not include an additional functional recitation added thereto which would bring 35 U.S.C. § 112 into consideration. With respect to apparatus claim 6, however, we agree with appellants that this claim must be construed in accordance with the requirements of 35 U.S.C. § 112. The statute requires that the means of a claim be interpreted to cover the corresponding structure described in the specification and equivalents thereof.

The only structure described in appellants' specification is a block diagram of a computer system as generally shown in Figure 1. A box 50 labeled "scheduler" is shown with a box 52 labeled "fast thread scheduler" contained therewithin. This is the only disclosed structure which corresponds to the scheduler of claim 6. The various means for selecting tasks to run in claim 6 and determining which path to follow are supported in the disclosure only by operating system kernel 12 and generic hardware system 14. The general block diagram shown in appellants' Figure 1 does not provide distinguishing

apparatus under 35 U.S.C. § 112 as argued by appellants. Appellants point to a description of the flow chart of Figures 3a and 3b, but this flow chart corresponds to a function or process being performed and not to a corresponding structure as required by the sixth paragraph of 35 U.S.C. § 112. Thus, even if appellants' claim 6 is properly construed in means plus function form, there is no corresponding structure disclosed which would patentably distinguish over the structure of Deitel's OS/2 computer system.

Since the facts of this case do not allow for any special claim construction under 35 U.S.C. § 112, we apply the general rule of claim construction. Claims are to be given their broadest reasonable interpretation during prosecution. In re Zletz, 893 F.2d 319, 321, 13 USPQ2d 1320, 1322 (Fed. Cir. 1989); In re Prater, 415 F.2d 1393, 1404, 162 USPQ 541, 550 (CCPA 1969). It is improper to narrow the scope of the claim by implicitly reading in disclosed limitations from the specification which have no express basis in the claims. See id. Using this general rule of claim construction, we agree with the examiner that the two paths of the claims are broad enough to be met by the regular path and the preemptive path of Deitel. Even though this may not be what appellants intended for their claims to cover, it is appellants' responsibility to limit the claim language to cover only that which they invented and not to cover prior art disclosures.

In summary, we have sustained the examiner's rejection of the claims under 35 U.S.C. § 102. Therefore, the decision of the examiner rejecting claims 1-8 is affirmed.

No time period for taking any subsequent action in connection with this appeal may be extended under 37 CFR § 1.136(a).

AFFIRMED

ERROL A. KRASS Administrative Patent Judge	)
JERRY SMITH Administrative Patent Judge	) BOARD OF PATENT) APPEALS AND) INTERFERENCES
JAMES T. CARMICHAEL Administrative Patent Judge	)

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